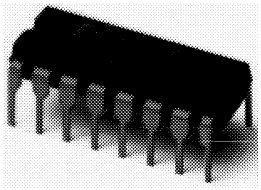
BURR - BROWN®



PCM61P

Serial Input 18-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

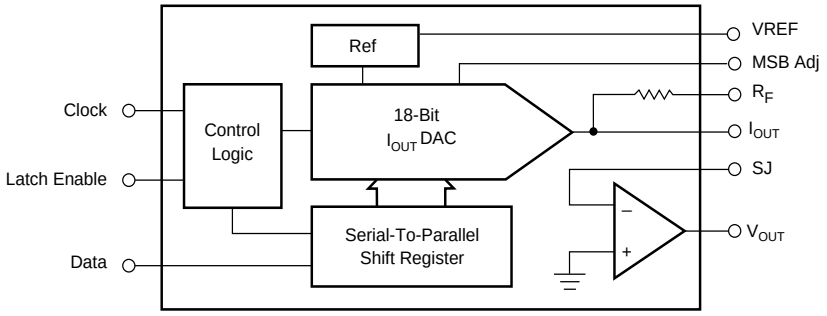
FEATURES

- **18-BIT MONOLITHIC AUDIO D/A CONVERTER**
- **LOW MAX THD + N: –92dB Without External Adjust**
- **100% PIN COMPATIBLE WITH INDUSTRY STD 16-BIT PCM56P**
- **LOW GLITCH OUTPUT OF ±3V OR ±1mA**
- **CAPABLE OF 8X OVERSAMPLING RATE IN V_{OUT} MODE**
- **COMPLETE WITH INTERNAL REFERENCE AND OUTPUT OP AMP**
- **RELIABLE PLASTIC 16-PIN DIP PACKAGE**

DESCRIPTION

The PCM61P is an 18-bit totally pin compatible performance replacement for the popular 16-bit PCM56P. With the addition of two extra bits, lower max THD+N (–92dB; PCM61P-K) can be achieved in audio applications already using the PCM56P. The PCM61P is complete with internal reference and output op amp and requires no external parts to function as an 18-bit DAC. The PCM61P is capable of an 8-times oversampling rate (single channel) and meets all of its specifications without an external output deglitcher.

The PCM61P comes in a small, reliable 16-pin plastic DIP package that has passed operating life tests under simultaneous high temperature, high humidity and high pressure testing.



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SPECIFICATIONS

ELECTRICAL

All specifications at 25°C, and $+V_{CC}$ = +5V, unless otherwise noted.

PARAMETER	CONDITIONS	PCM61P-P, J-P, K MIN	PCM61P-P, J-P, K TYP	PCM61P-P, J-P, K MAX	UNITS
RESOLUTION				18	Bits
DYNAMIC RANGE			108		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}		+2.4		$+V_L$	V
V_{IL}		0		+0.8	V
I_{IH}	V_{IH} = +2.7V			+1	µA
I_{IL}	V_{IL} = +0.4V			–50	µA
Data Format		Serial BTC[1]			
Input Clock Frequency				16.9	MHz
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion + N[2]	Without MSB Adjustments				
PCM61P					
f = 991Hz (0dB)[3]	f_S = 176.4kHz[4]		–88	–82	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–74	–68	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–34	–28	dB
PCM61P-J					
f = 991Hz (0dB)	f_S = 176.4kHz		–94	–88	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–76	–74	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–36	–34	dB
PCM61P-K					
f = 991Hz (0dB)	f_S = 176.4kHz		–98	–92	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–80	–74	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–40	–34	dB
IDLE CHANNEL SNR	20Hz to 20kHz at BPZ[5]		112		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±2		%FSR
Bipolar Zero Error			±30		mV
Differential Linearity Error			±0.001		%FSR
Total Drift[6]	0°C to 70°C		±25		ppm of FSR/°C
Bipolar Zero Drift	0°C to 70°C		±4		ppm of FSR/°C
Warm-up Time		1			Minute
MONOTONICITY			16		Bits
ANALOG OUTPUT					
Voltage: Output Range			±3		V
Output Current		±2			mA
Output Impedance			0.1		Ω
Current: Output Range	±30%		±1		mA
Output Impedance	±30%		1.2		kΩ
SETTLING TIME	To ±0.006% of FSR				
Voltage: 6V Step			1.5		µs
1 LSB			1.0		µs
Slew Rate			12		V/µs
Current: 1mA Step	10Ω to 100Ω Load		250		ns
1mA Step	1kΩ Load		350		ns
Glitch Energy	Meets all THD+N specs without external deglitching				
POWER SUPPLY REQUIREMENTS[7]					
$\pm V_{CC}$ Supply Voltage		±4.75	±5	±13.2	V
Supply Current: $+I_{CC}$	$+V_{CC}$ = +5V		+10	+17	mA
$+I_{CC}$	$+V_{CC}$ = +12V		+12		mA
$-I_{CC}$	$-V_{CC}$ = –5V		–25	–35	mA
$-I_{CC}$	$-V_{CC}$ = –12V		–27		mA
Power Dissipation	$\pm V_{CC}$ = ±5V		175	260	mW
	$\pm V_{CC}$ = ±12V		475		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–30		+70	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$)/$Signal_{RMS}$. (3) D/A converter output frequency/signal level. (4) D/A converter sample frequency (4 x 44.1kHz; 4 times oversampling). (5) Bipolar zero, using A-weighted filter. (6) This is the combined drift error due to gain, offset, and linearity over temperature. (7) All positive and all negative supply pins must be tied together respectively.

PIN ASSIGNMENTS

PIN	FUNCTION	DESCRIPTION
1	$-V_S$	Analog Negative Supply
2	LOG COM	Logic Common
3	$+V_L$	Logic Positive Supply
4	NC	No Connection
5	CLK	Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Supply
9	V_{OUT}	Voltage Output
10	RF	Feedback Resistance
11	SJ	Summing Junction
12	ANA COM	Analog Common
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trim-pot Terminal
16	$+V_S$	Analog Positive Supply

ABSOLUTE MAXIMUM RATINGS

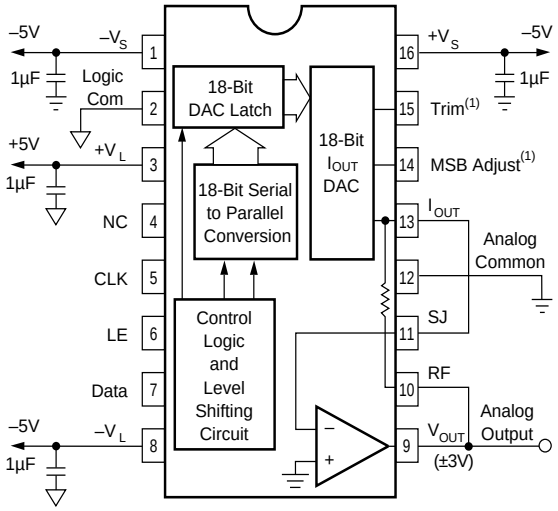
DC Supply Voltages ..... ±16VDC
Input Logic Voltage ..... –1V to V_S /$+V_L$
Power Dissipation 850mW
Operating Temperature Range ..... –25°C to +70°C
Storage Temperature Range ..... –60°C to +100°C
Lead Temperature (soldering, 10s) ..... +300°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM61P-P	16-Pin Plastic DIP	180
PCM61P-J	16-Pin Plastic DIP	180
PCM61P-K	16-Pin Plastic DIP	180

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

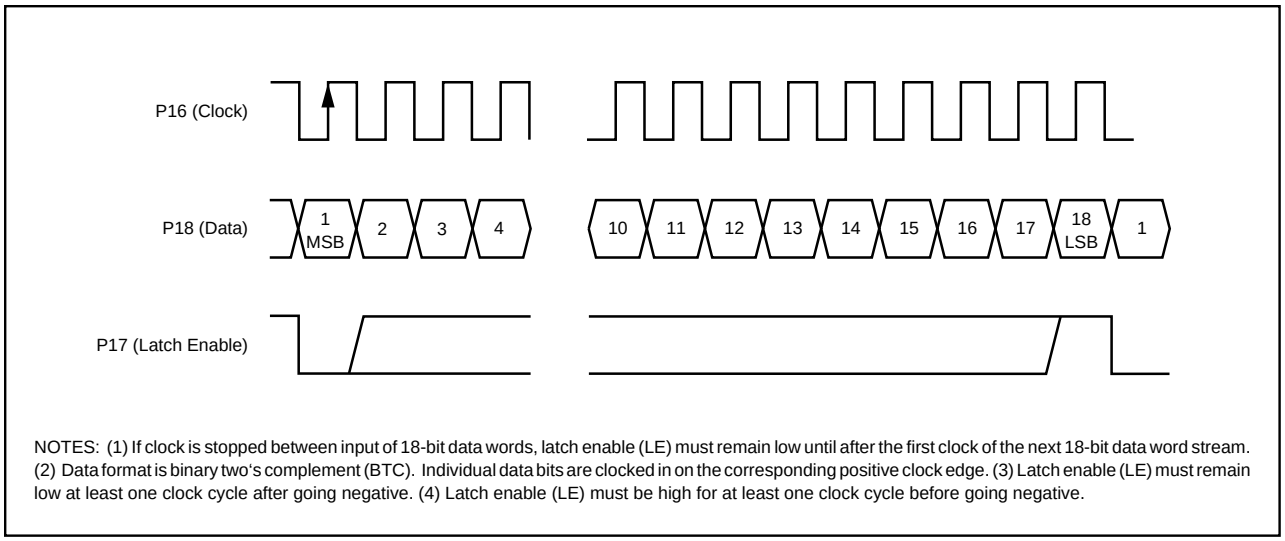
CONNECTION DIAGRAM



NOTE: (1) MSB error (Bipolar Zero differential linearity error) can be adjusted to zero using the external circuit shown in Figure 4.

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V) V_{OUT} Mode	Current (mA) I_{OUT} Mode
1FFFF Hex	+FS	–0.99999237	+2.99997711
00000 Hex	BPZ	0.00000000	0.00000000
3FFFF Hex	BPZ – 1LSB	+0.00000763	–0.00002289
20000 Hex	–FS	+1.00000000	–3.00000000

TABLE I. PCM61P Input/Output Relationships.



NOTES: (1) If clock is stopped between input of 18-bit data words, latch enable (LE) must remain low until after the first clock of the next 18-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 1. PCM61P Timing Diagram.

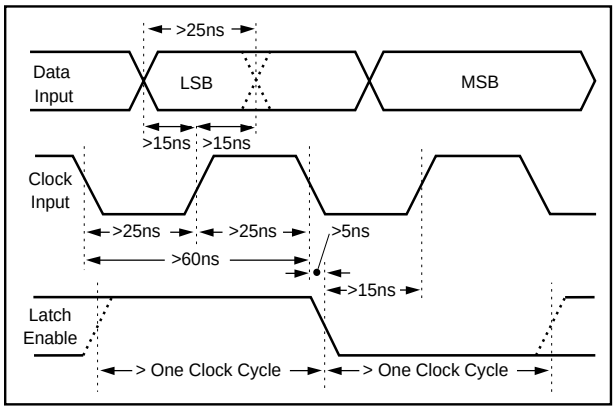


FIGURE 2. PCM61P Setup and Hold Timing Diagram.

MAXIMUM CLOCK RATE

The maximum clock rate of 16.9MHz for the PCM61P is derived by multiplying the standard audio sample rate of 44.1kHz times sixteen (16 x oversampling) times the standard audio word bit length of 24 (44.1kHz x 16 x 24 = 16.9MHz). Note that this clock rate accommodates a 24-bit word length, even though only 18 bits are actually being used.

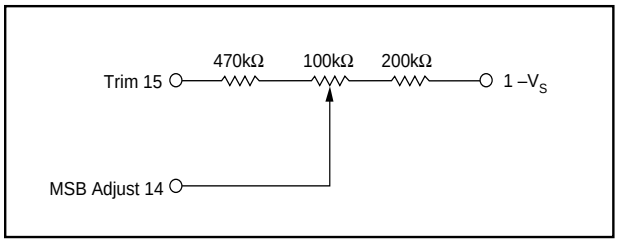


FIGURE 3. MSB Adjust Circuit.

MSB ERROR ADJUSTMENT PROCEDURE (OPTIONAL)

The MSB error of the PCM61P can be adjusted to make the differential linearity error (DLE) at BPZ essentially zero. This is important when the signal output levels are very low, because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small code changes occurring in the LSB portion of the converter.

To statically adjust DLE at BPZ, refer to the circuit shown in Figure 3 or the PCM61P connection diagram.

Differential linearity error at bipolar zero and THD are guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point, which makes it possible to eliminate DLE error at BPZ. Two procedures are given to allow either static or dynamic adjustment. The dynamic procedure is preferred because of the difficulty associated with the static method (accurately measuring 16-bit LSB steps).

After allowing ample warm-up time (5-10 minutes) to assure stable operation of the PCM61P, select input code 3FFFF hexadecimal (all bits on except the MSB). Measure the output voltage using a 6-1/2 digit voltmeter and record it. Change the digital input code to 00000 hexadecimal (all bits off except the MSB). Adjust the 100kΩ potentiometer to make the output read 22.9μV more than the voltage reading of the previous code (a 1LSB step = 22.9μV). A much simpler method is to dynamically adjust the DLE at BPZ. Assuming the device has been installed in a digital audio application circuit, send the appropriate digital input to produce a –60dB level sinusoidal output, then adjust the 100kΩ potentiometer until a minimum level of distortion is observed.